FORM 6-K

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

For the month November 2025 No. 2

TOWER SEMICONDUCTOR LTD.

(Translation of registrant's name into English)

Ramat Gavriel Industrial Park
P.O. Box 619, Migdal Haemek, Israel 2310502
(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover Form 20-F or Form 40-F.

Form 20-F ☒ Form 40-F ☐

Indicate by check mark whether the registrant by furnishing the information contained in this Form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.

Yes ☐ No ☒

On November 12, 2025, the Registrant Announces New CPO Foundry Technology Available on Tower's Leading Sipho and EIC Optical Platforms

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

TOWER SEMICONDUCTOR LTD.

Date: November 12, 2025

By: /s/ Nati Somekh
Name: Nati Somekh
Title: Corporate Secretary

Tower Semiconductor Announces New CPO Foundry Technology Available on Tower's Leading Sipho and EIC Optical Platforms

Leveraging years of stacked BSI sensor production, Tower's wafer-scale 3D-IC technology unlocks integration of SiPho and EIC processes for emerging applications such as Co-Packaged Optics, including full support by Cadence design tools to the stacked platform technology

Migdal Haemek, Israel – November 12, 2025 – Tower Semiconductor (NASDAQ/TASE: TSEM), a leading foundry of high-value analog semiconductor solutions, today announced the expansion of its existing, mature 300mm wafer bonding technology, originally developed and in mass production for stacked BSI image sensors, to enable heterogeneous 3D-IC integration across its industry-leading Silicon Photonics (SiPho) and SiGe BiCMOS processes, including full support by Cadence design tools for the stacked platform technology. The new offering, represents a major step forward in extending wafer-scale 3D integration, requiring simultaneous use of multiple-PDKs, to new domains beyond image sensing, addressing the growing market demand for compact, high-performance systems for data center applications.

Building on years of high-volume stacked sensor production on 200mm and 300mm wafers, Tower's wafer bonding technology enables stacking wafers (for example, SiPho (PIC - Photonic IC) and SiGe (EIC - Electronic IC)) to create fully integrated 3D-ICs at the wafer scale. This capability integrates application-specific functions from different process technologies into a single high-density chip, delivering greater functionality and performance in a smaller form factor. This wafer-scale 3D-IC technology supports emerging applications such as Co-Packaged Optics (CPO), which combines PICs and EICs, where compact, high-performance integration is essential.

"Our long-standing experience in high-volume wafer stacking for CIS technologies has laid the foundation for this next stage of 3D integration," **said Dr. Marco Racanelli, President, Tower Semiconductor.** "With our advanced 300 mm wafer bonding process now supporting multiple wafer technologies on a single 3D-IC, we are enabling customers to achieve new levels of performance, functionality, and integration density needed for CPO."

Tower has already successfully demonstrated the wafer bonding process's precision alignment and reliability. Complementing the process technology, Tower has collaborated with Cadence Design Systems to extend their Virtuoso Studio Heterogeneous Integration flow – which allows co-simulation and co-verification of multiple process technologies within a unified design environment. This enhanced design enablement capability is now available for our customers to use as a reference flow.

"Tower Semiconductor and Cadence have joined forces to provide a comprehensive design flow for multi-technology stacked die," **said Dr. Samir Chaudhry, VP of Customer Design Enablement**, **Tower Semiconductor**. "This enables designers to lay out, check connectivity, and fully simulate 3D-IC and wafer-bonded chips built from multiple technology platforms, all within a single Cadence design project. Compatible with Tower Semiconductor SiGe BiCMOS and SiPho PDKs, - the new 3D-IC design flow is now fully supported by both companies, greatly improving first-pass success on complex multi-technology die projects."

"Cadence and Tower have successfully collaborated for over two decades, helping our mutual analog IC customers achieve first pass success with their complex designs", **said Ashutosh Mauskar, VP, Product Management for the Custom Design and System Design and Analysis products, Cadence**. "The validation of the Heterogeneous Integration flow, which supports die-to-wafer and wafer-to-wafer applications for PIC/EIC sub-systems using Tower technology, means our mutual customers can count on a robust and unified technology flow to help them deliver quality products on time."

This expansion reinforces Tower's leadership in 3D-IC and heterogeneous integration, delivering advanced analog solutions that accelerate innovation across next-generation markets.

For additional information about the company's technology platforms, visit here.

About Tower Semiconductor

Tower Semiconductor Ltd. (NASDAQ/TASE: TSEM), the leading foundry of high-value analog semiconductor solutions, provides technology, development, and process platforms for its customers in growing markets such as consumer, industrial, automotive, mobile, infrastructure, medical and aerospace and defense. Tower Semiconductor focuses on creating a positive and sustainable impact on the world through long-term partnerships and its advanced and innovative analog technology offering, comprised of a broad range of customizable process platforms such as SiGe, BiCMOS, mixed-signal/CMOS, RF CMOS, CMOS image sensor, non-imaging sensors, displays, integrated power management (BCD and 700V), photonics, and MEMS. Tower Semiconductor also provides world-class design enablement for a quick and accurate design cycle as well as process transfer services including development, transfer, and optimization, to IDMs and fabless companies. To provide multi-fab sourcing and extended capacity for its customers, Tower Semiconductor owns one operating facility in Israel (200mm), two in the U.S. (200mm), two in Japan (200mm and 300mm) which it owns through its 51% holdings in TPSCo, shares a 300mm facility in Agrate, Italy with STMicroelectronics as well as has access to a 300mm capacity corridor in Intel's New Mexico factory. For more information, please visit: www.towersemi.com.

Safe Harbor Regarding Forward-Looking Statements

This press release includes forward-looking statements, which are subject to risks and uncertainties. Actual results may vary from those projected or implied by such forward-looking statements. A complete discussion of risks and uncertainties that may affect the accuracy of forward-looking statements included in this press release or which may otherwise affect Tower's business is included under the heading "Risk Factors" in Tower's most recent filings on Forms 20-F, F-3, F-4 and 6-K, as were filed with the Securities and Exchange Commission (the "SEC") and the Israel Securities Authority. Tower does not intend to update, and expressly disclaim any obligation to update, the information contained in this release.

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