

FORM 6-K

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

For the month of November 2004 No. 3

TOWER SEMICONDUCTOR LTD.
(Translation of registrant's name into English)

P.O. BOX 619, MIGDAL HAEMEK, ISRAEL 23105
(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover Form 20-F or Form 40-F.

Form 20-F Form 40-F

Indicate by check mark whether the registrant by furnishing the information contained in this Form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.

Yes No

On November 17, 2004, the Registrant announced expansion of its foundry solutions portfolio with 0.16-micron optical shrink that provides lower die cost to customers and yields higher wafer prices. Attached hereto is a copy of the press release.

This Form 6-K is being incorporated by reference into all effective registration statements filed by us under the Securities Act of 1933.

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

TOWER SEMICONDUCTOR LTD.

Date: November 17, 2004

By: /s/ Tamar Cohen

Tamar Cohen
Corporate Secretary

TOWER SEMICONDUCTOR EXPANDS FOUNDRY SOLUTIONS PORTFOLIO
WITH 0.16-MICRON OPTICAL SHRINK

NEW PROCESS IMPROVES TOWER'S COMPETITIVE POSITION

0.16-MICRON PROVIDES LOWER DIE COST TO CUSTOMERS WHILE YIELDS HIGHER
WAFER PRICES

MIGDAL HAEMEK, ISRAEL, NOVEMBER 17, 2004 - Tower Semiconductor Ltd. (NASDAQ:TSEM, TASE:TSEM), a pure-play independent wafer foundry announced today that in response to its customer's demand, it is introducing a 0.16-micron optical shrink solution. The offering represents a 10% linear shrink from Tower's existing 0.18-micron offering while utilizing virtually the same 0.18-micron libraries and IP. The shrink allows both Tower and its customers to benefit from a 15 to 20 percent die size reduction through a potentially higher wafer ASP and lower die cost.

"With our cost-effective 0.16-micron device solution, we are able to maintain the same design environment as 0.18-micron and make the required conversions while reducing the customer burden of designer-to-foundry interaction," said Doron Simon, president of Tower Semiconductor USA. "This translates to significant value for our existing customers while increasing our competitiveness in the marketplace."

The offering is tailored to customers who are looking to achieve cost reduction at the 0.18-micron technology node. Applications include industry standard CMOS logic and mixed-signal technologies. The 0.16-micron optical shrink solution is qualified and production ready. For customers looking to prototype their designs, the solution is available on the Tower Shuttle Program.

ABOUT TOWER SEMICONDUCTOR LTD.

Tower Semiconductor LTD. is a pure-play independent wafer foundry established in 1993. The company manufactures integrated circuits with geometries ranging from 1.0 to 0.13 micron; it also provides complementary technical services and design support. In addition to digital CMOS process technology, Tower offers advanced non-volatile memory solutions, mixed-signal and CMOS image-sensor technologies. To provide world-class customer service, the company maintains two manufacturing facilities: Fab 1 has process technologies from 1.0 to 0.35 micron and can produce up to 16,000 150mm wafers per month. Fab 2 features 0.18-micron and below process technologies, including foundry-standard technology. When complete, Fab 2 is expected to offer full production capacity of 33,000 200mm wafers per month. The Tower Web site is located at www.towersemi.com.

SAFE HARBOR

THIS PRESS RELEASE INCLUDES FORWARD-LOOKING STATEMENTS, WHICH ARE SUBJECT TO RISKS AND UNCERTAINTIES. ACTUAL RESULTS MAY VARY FROM THOSE PROJECTED OR IMPLIED BY SUCH FORWARD-LOOKING STATEMENTS. POTENTIAL RISKS AND UNCERTAINTIES INCLUDE, WITHOUT LIMITATION, RISKS AND UNCERTAINTIES ASSOCIATED WITH: (I) THE COMPLETION OF THE EQUIPMENT INSTALLATION, TECHNOLOGY TRANSFER AND RAMP-UP OF PRODUCTION IN FAB 2, (II) HAVING SUFFICIENT FUNDS TO COMPLETE THE FAB 2 PROJECT, (III) THE CYCLICAL NATURE OF THE SEMICONDUCTOR INDUSTRY AND THE RESULTING PERIODIC OVERCAPACITY, (IV) OPERATING OUR FACILITIES AT SATISFACTORY UTILIZATION RATES, (V) THE EFFECT THAT OUR EXPECTED DECREASE IN SALES IN THE COMING QUARTERS WILL HAVE ON OUR ABILITY TO MEET CERTAIN OF THE COVENANTS STIPULATED IN OUR AMENDED FACILITY AGREEMENT, WHICH WE CURRENTLY FORECAST WE WILL NOT MEET IN THE NEXT SEVERAL QUARTERS, (VI) OUR ABILITY TO CAPITALIZE ON INCREASES IN DEMAND FOR FOUNDRY SERVICES, (VII) MEETING THE CONDITIONS TO RECEIVE ISRAELI GOVERNMENT GRANTS AND TAX BENEFITS APPROVED FOR FAB 2, WHICH WE CURRENTLY FORECAST WE MAY NOT MEET, AND OBTAINING THE APPROVAL OF THE ISRAELI INVESTMENT CENTER TO EXTEND THE FIVE-YEAR INVESTMENT PERIOD UNDER OUR FAB 2 APPROVED ENTERPRISE PROGRAM, (VIII) ATTRACTING ADDITIONAL CUSTOMERS, (IX) NOT RECEIVING ORDERS FROM OUR WAFER PARTNERS AND TECHNOLOGY PROVIDERS, (X) FAILING TO MAINTAIN AND DEVELOP OUR TECHNOLOGY PROCESSES AND SERVICES, (XI) COMPETING EFFECTIVELY, (XII) OUR LARGE AMOUNT OF DEBT, AND (XIII) ACHIEVING ACCEPTABLE DEVICE YIELDS, PRODUCT PERFORMANCE AND DELIVERY TIMES. A MORE COMPLETE DISCUSSION OF RISKS AND UNCERTAINTIES THAT MAY AFFECT THE ACCURACY OF FORWARD-LOOKING STATEMENTS INCLUDED IN THIS PRESS RELEASE OR WHICH MAY OTHERWISE AFFECT OUR BUSINESS IS INCLUDED UNDER THE HEADING "RISK FACTORS" IN OUR MOST RECENT ANNUAL REPORT ON FORM 20-F AND IN OUR FORM F-3, AS AMENDED, AS WERE FILED WITH THE SECURITIES AND EXCHANGE COMMISSION AND THE ISRAEL SECURITIES AUTHORITY.

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